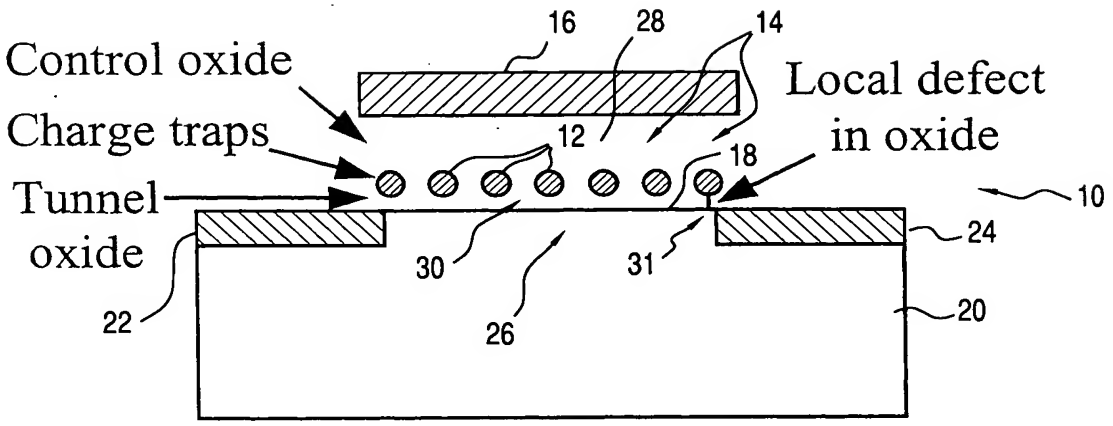
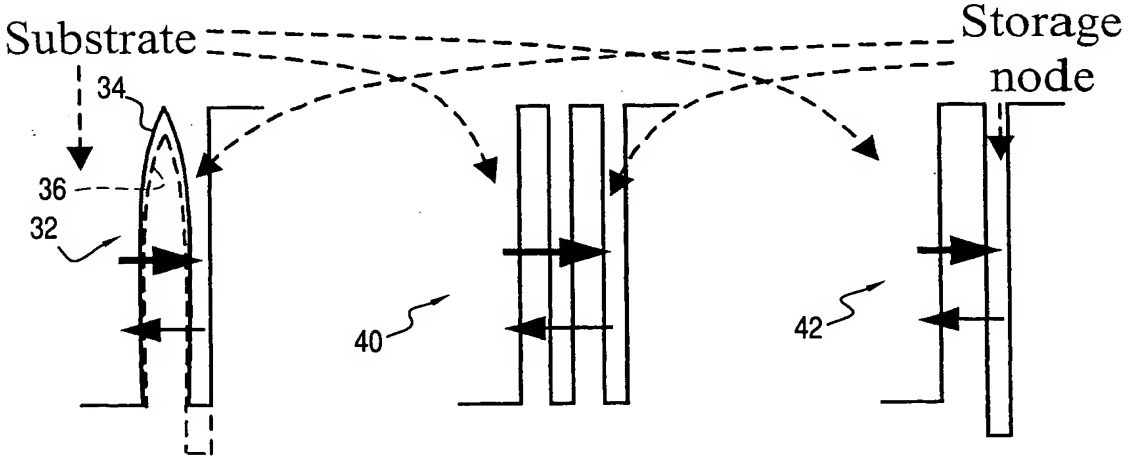


FIG. 1(a)



Dielectric Engineering

FIG. 1(b)

Double-stack storage nodes

FIG. 1(c)

Work function Engineering

FIG. 1(d)

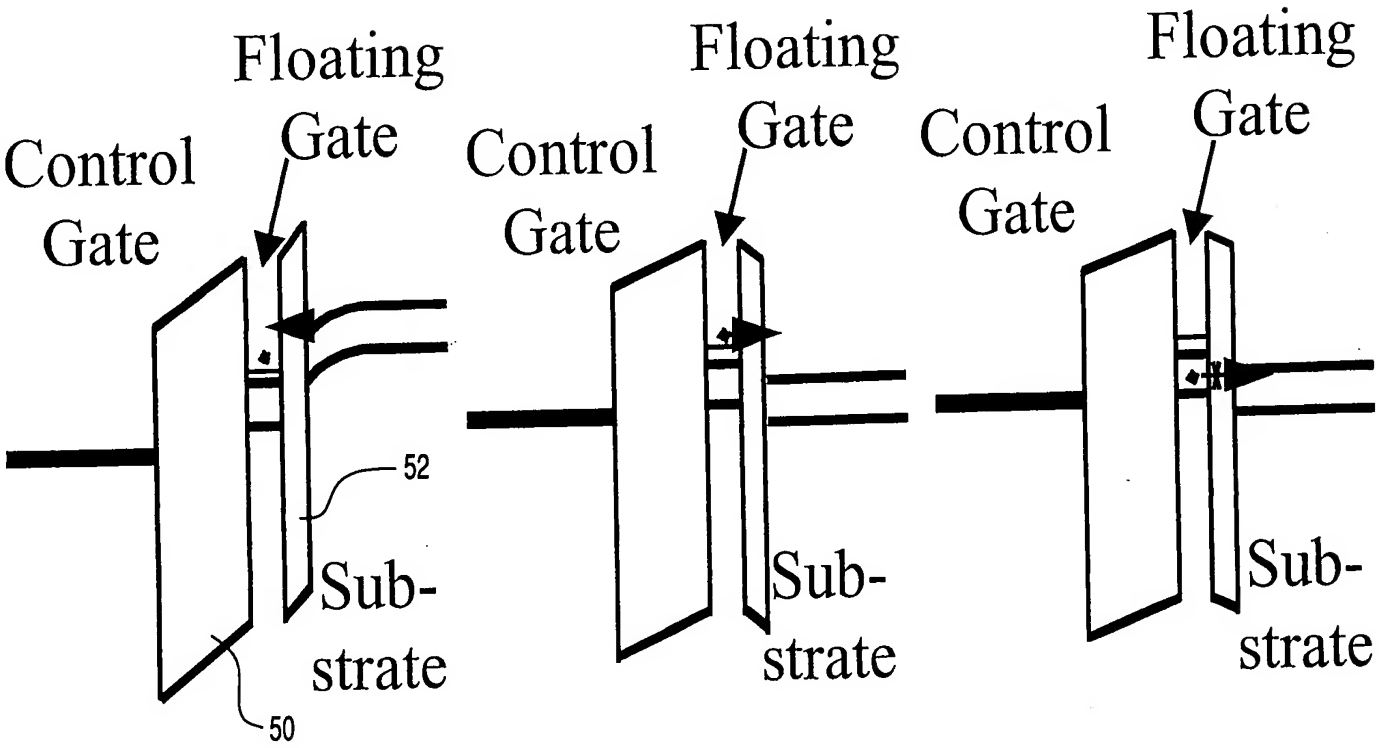


FIG. 2(a)
(writing)

FIG. 2(b)
(retention)

FIG. 2(c)
(retention)

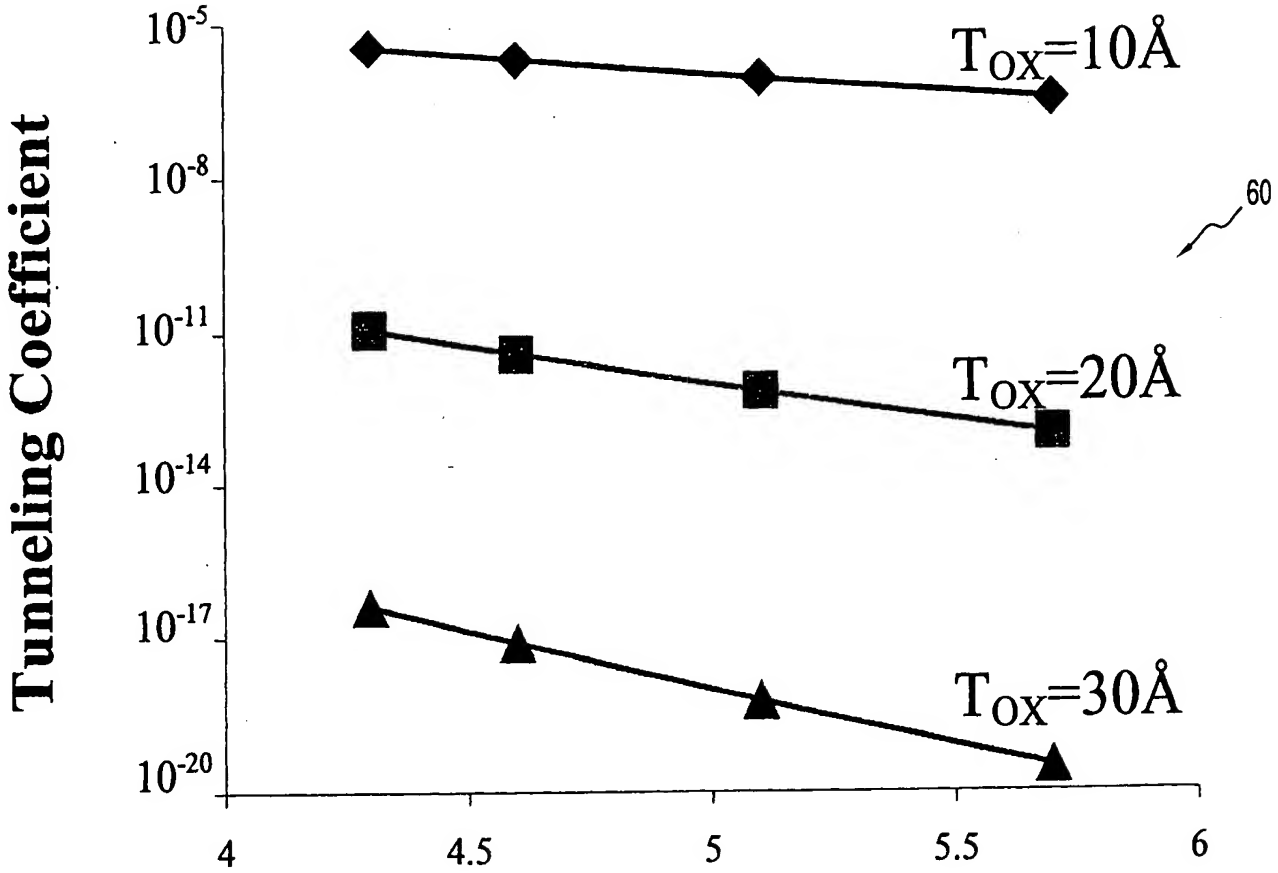


FIG. 3

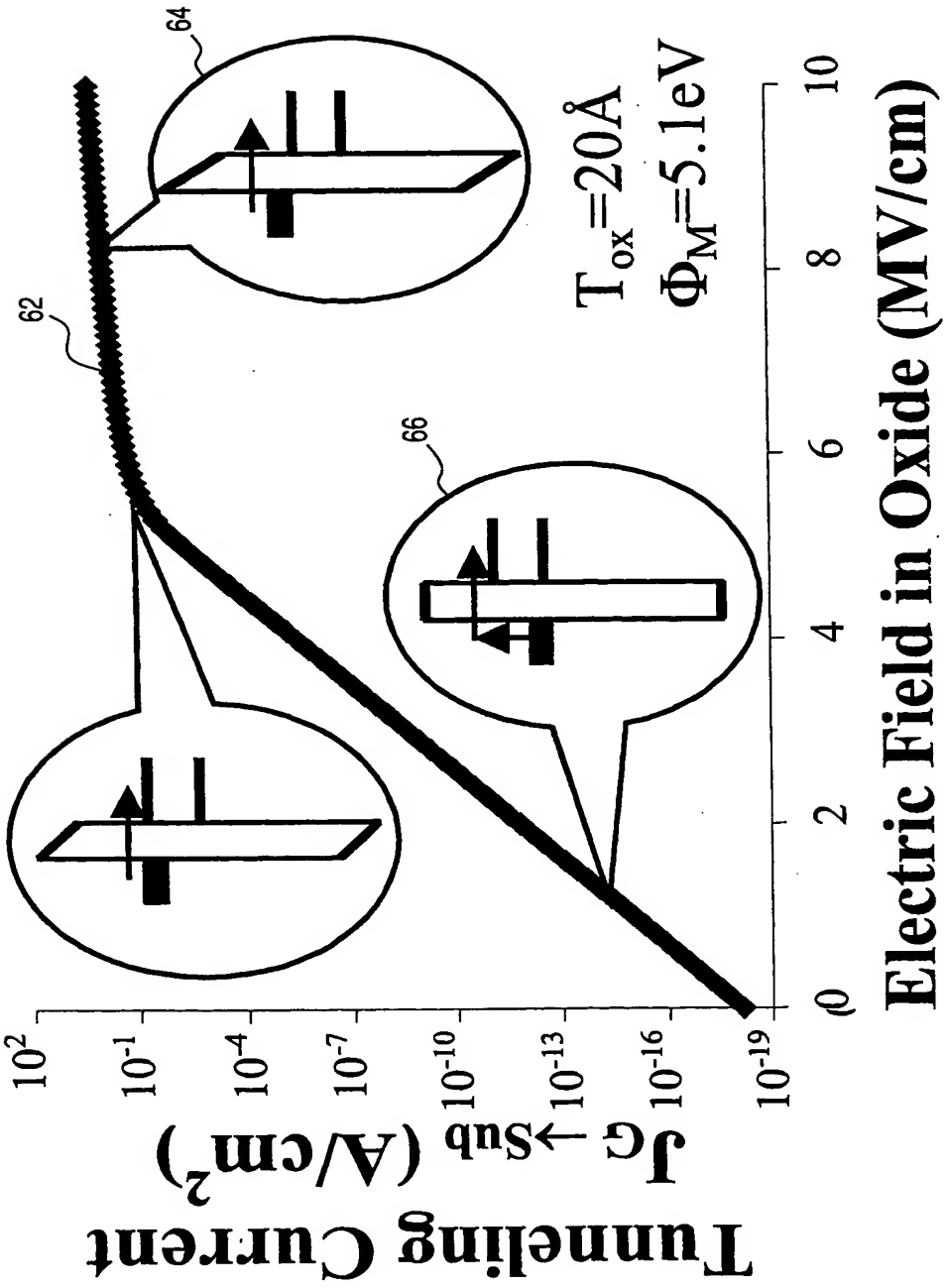


FIG. 4

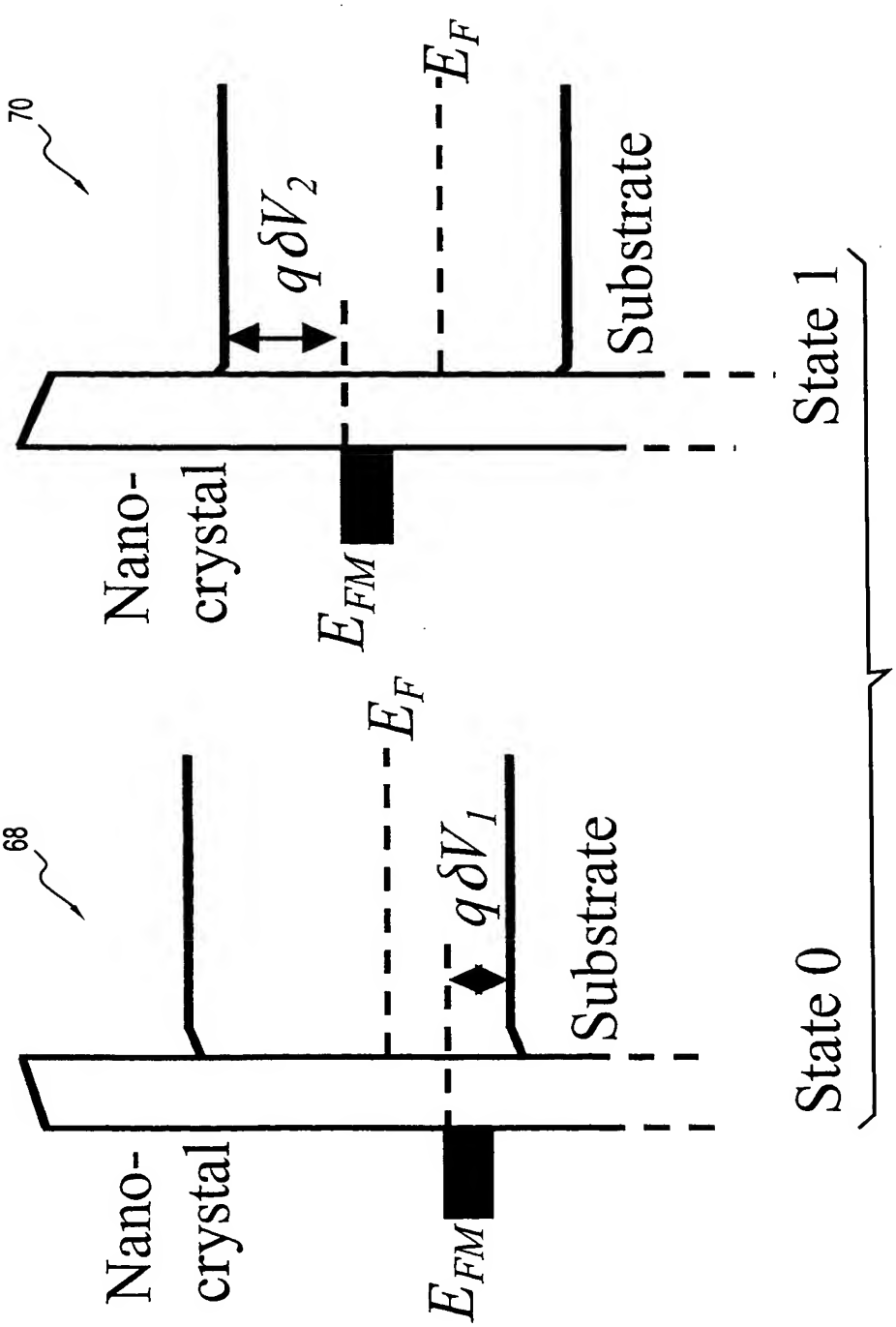


FIG. 5

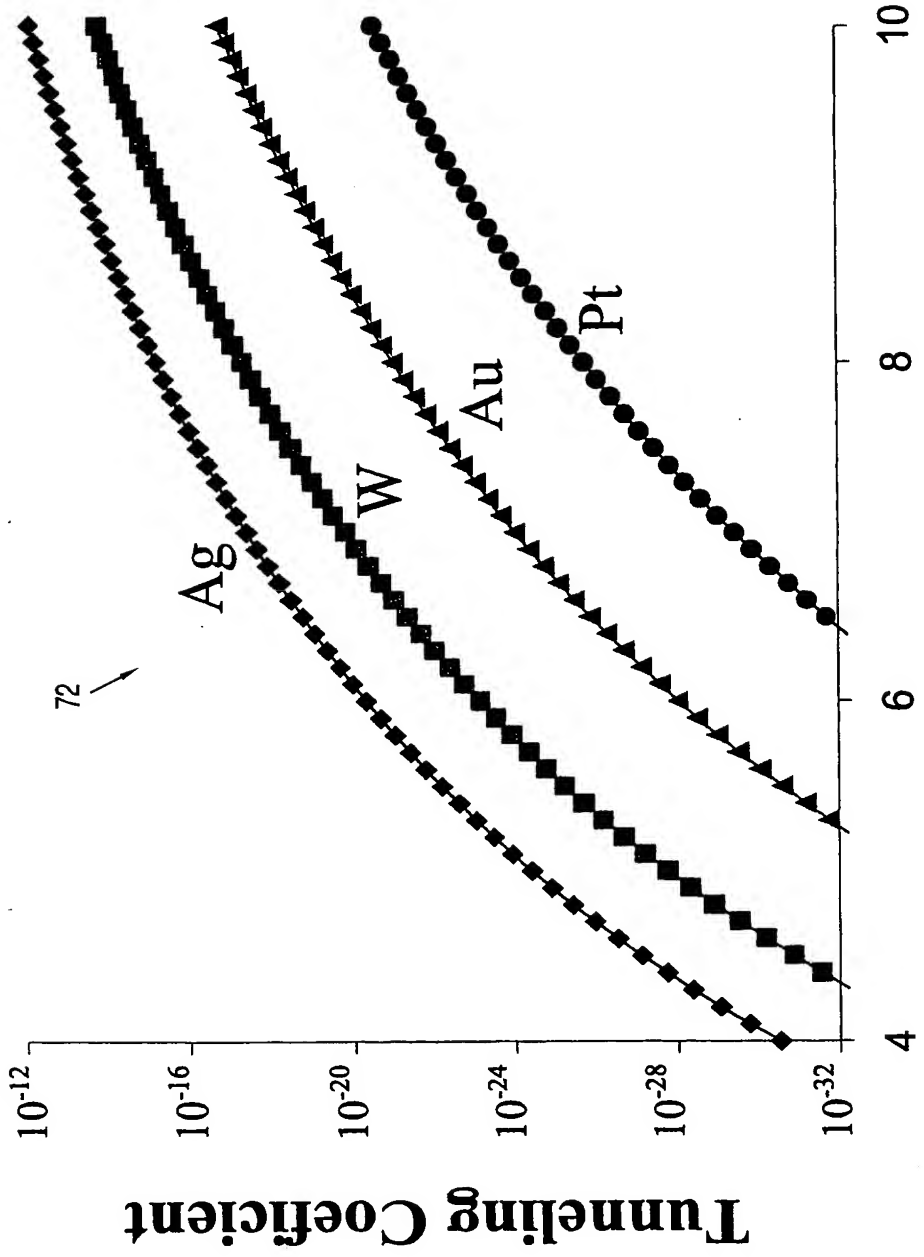


FIG. 6

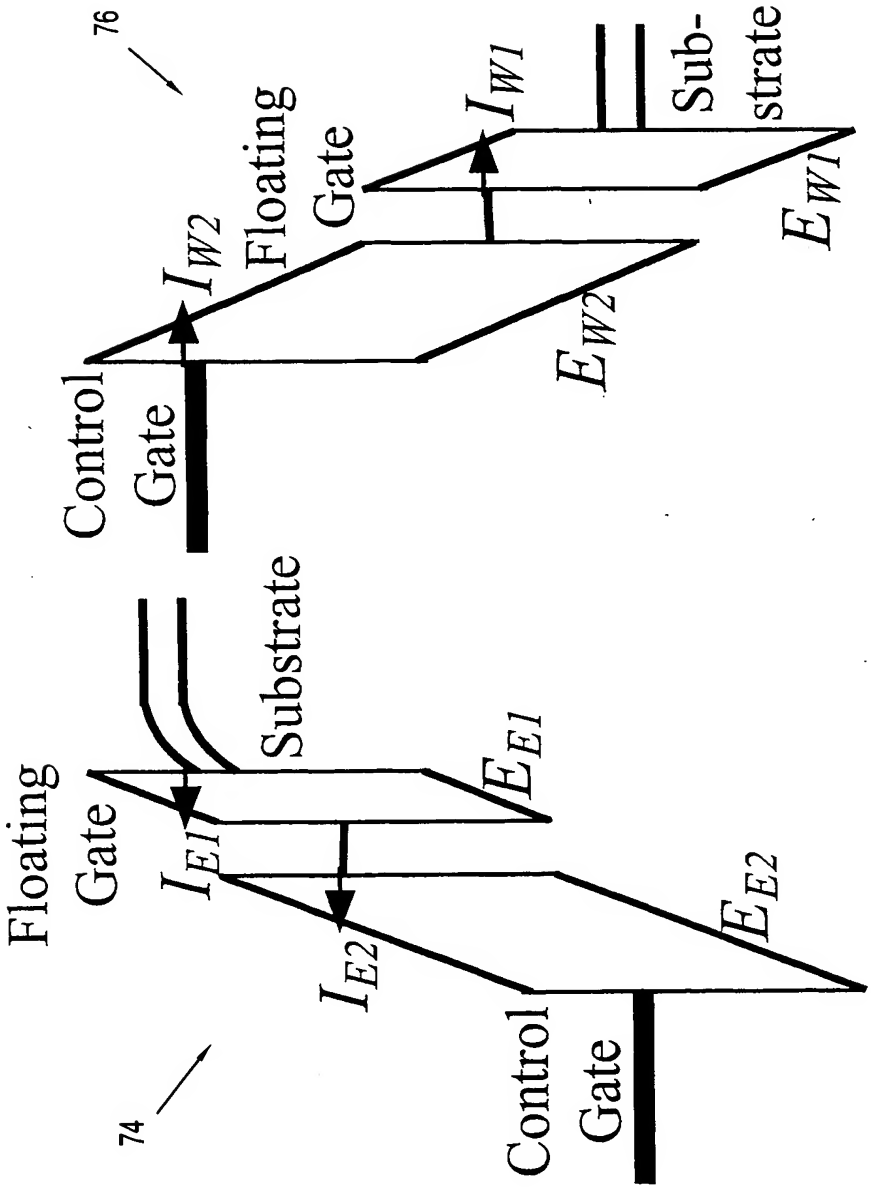


FIG. 7

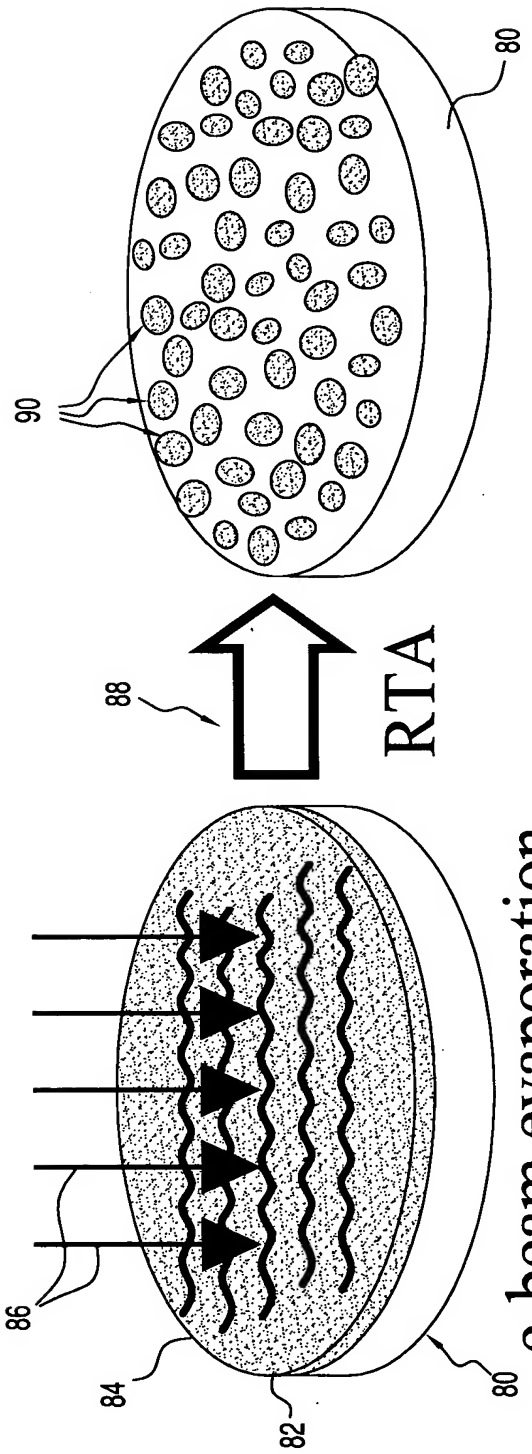


FIG. 8

FIG. 9

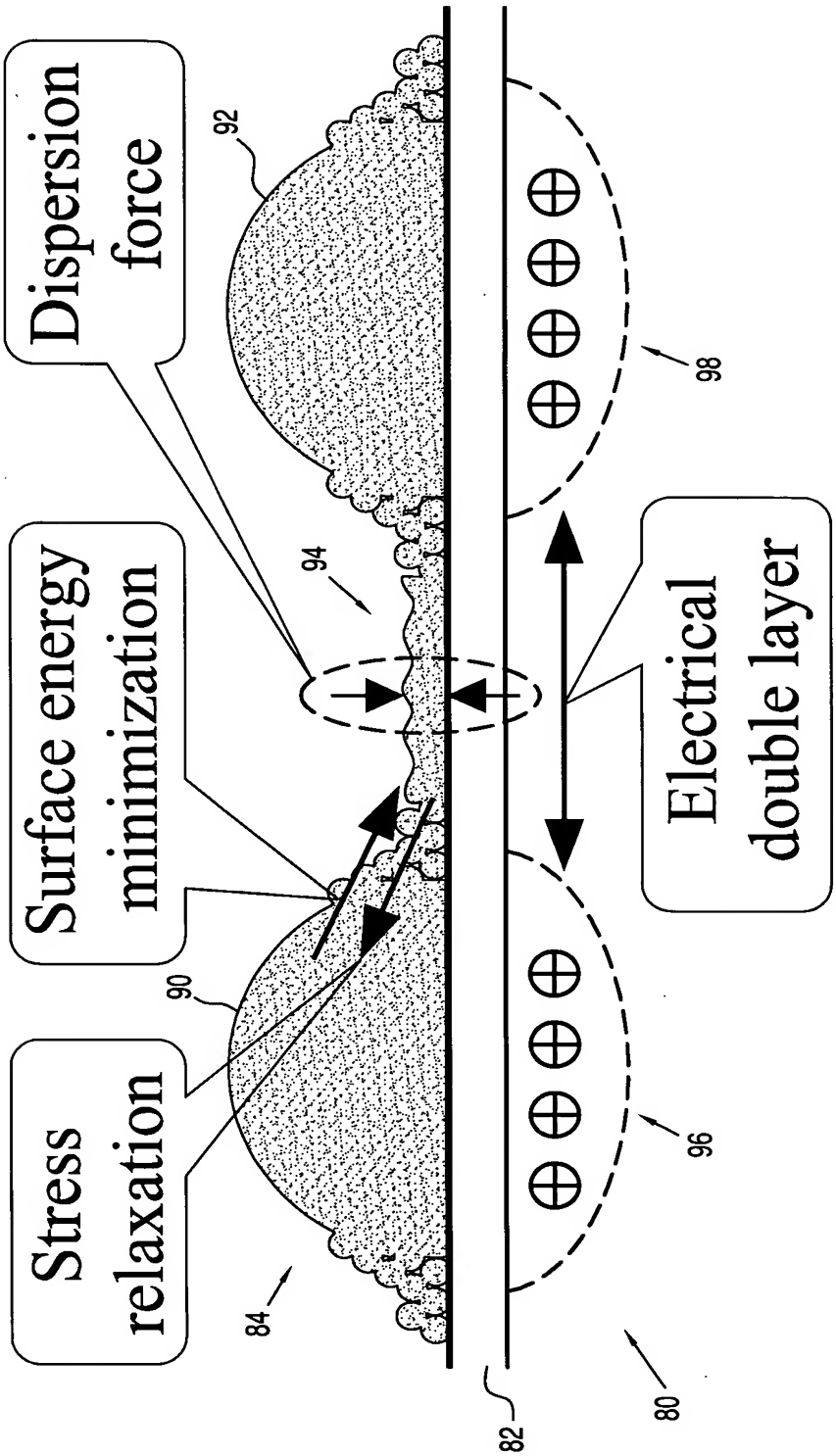


FIG. 10(a)

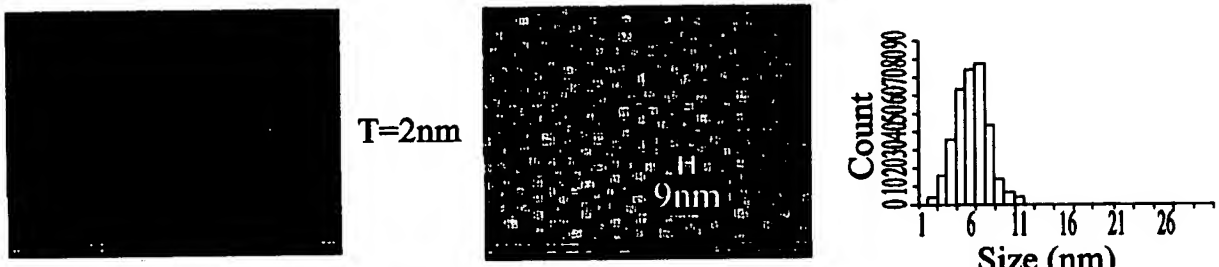


FIG. 10(b)

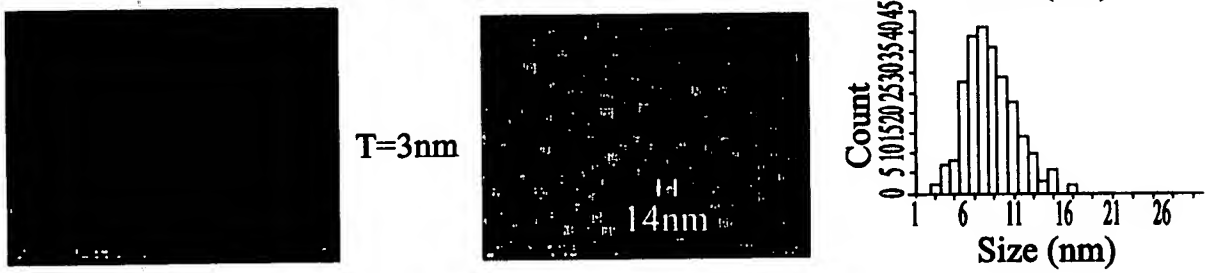


FIG. 10(c)

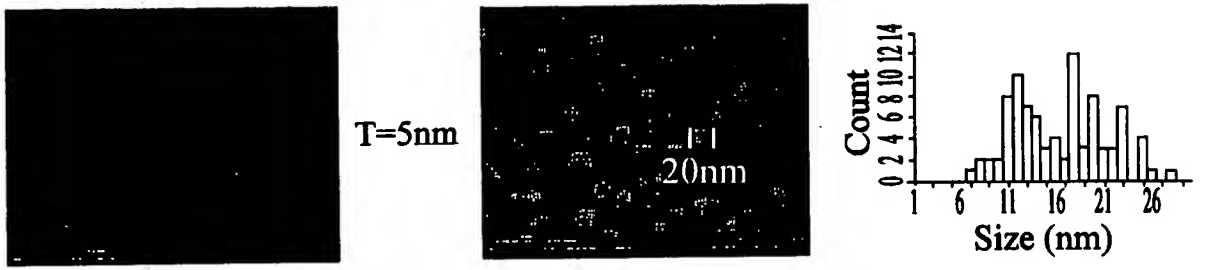
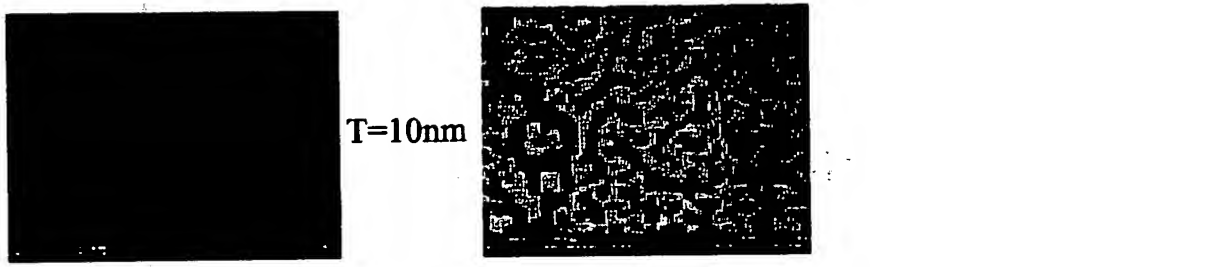


FIG. 10(d)

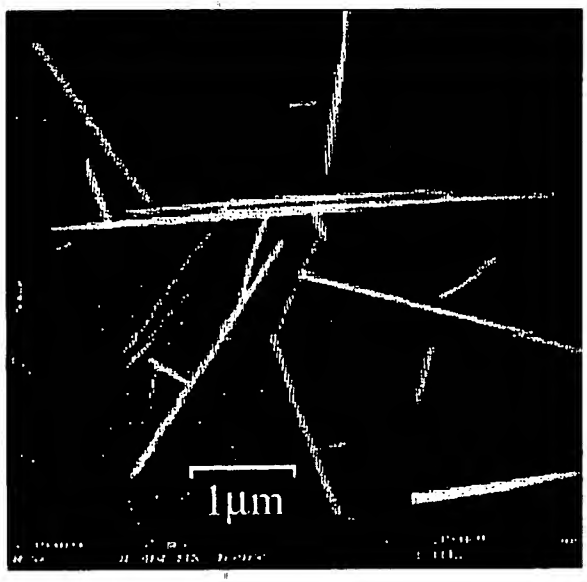


Before RTA

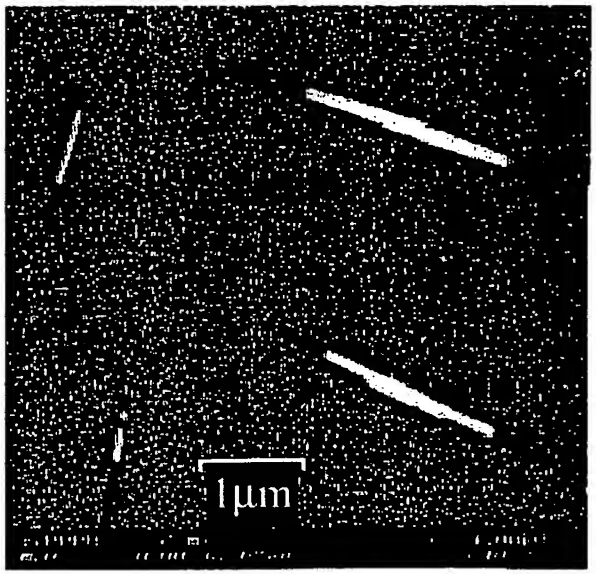
After RTA

Size Distribution

FIG. 11(a)



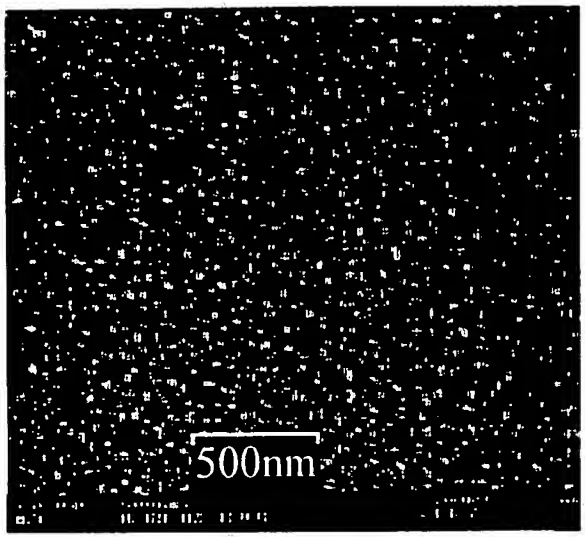
RTA at 950°C, 2 minutes



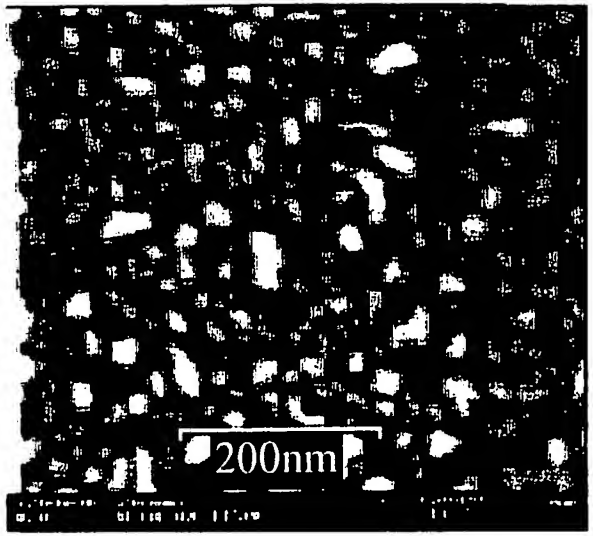
RTA at 1000°C, 2 minutes

FIG. 11(b)

FIG. 11(c)



RTA at 1050°C, 2 minutes



RTA at 1100°C, 2 minutes

FIG. 11(d)

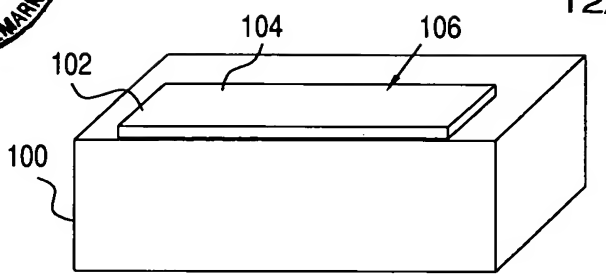


FIG. 12(a)
Definition of active region

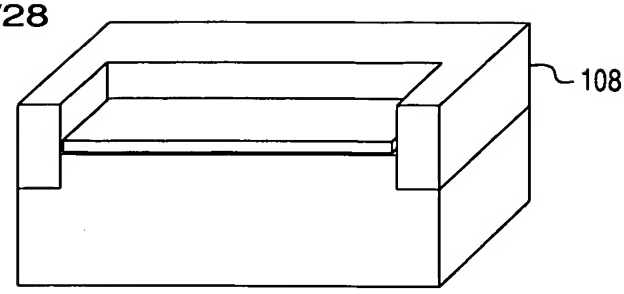


FIG. 12(b)
1 μm field oxidation

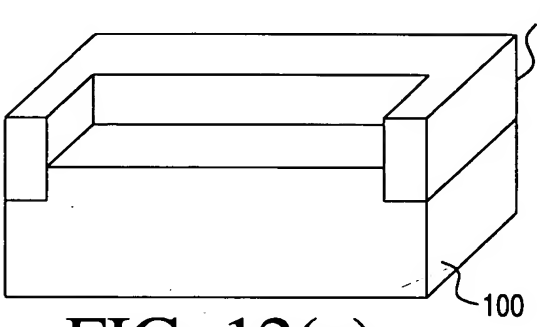


FIG. 12(c)
Stripping nitride and pad oxide layers

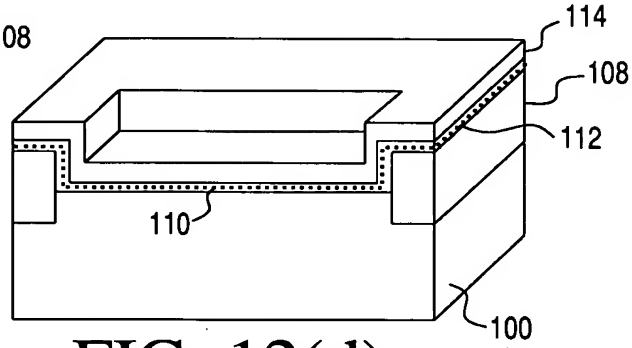


FIG. 12(d)
Gate stack formation

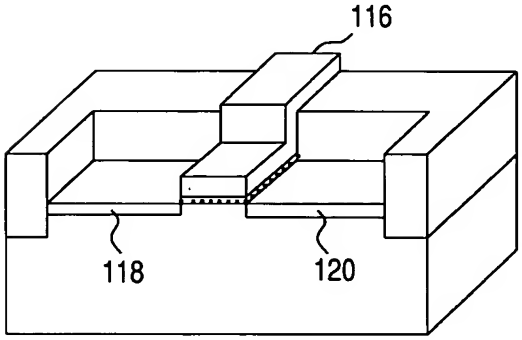


FIG. 12(e)
Definition of gate pattern followed by S/D ion implantation

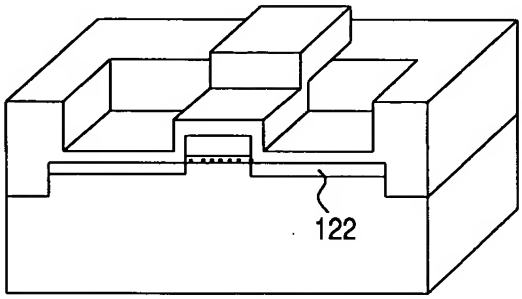


FIG. 12(f)
PECVD oxide deposition for isolation between gate and S/D

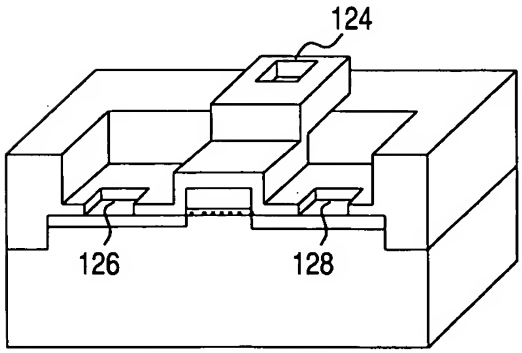


FIG. 12(g)
Etching contact window

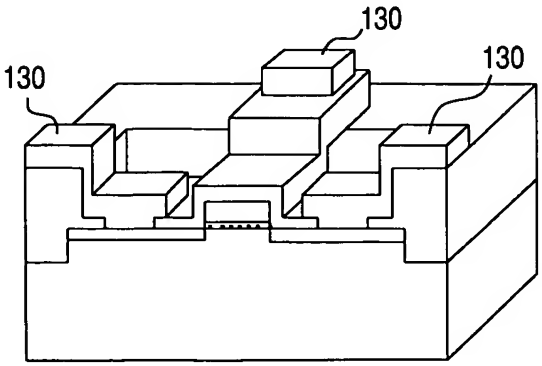


FIG. 12(h)
W sputtering and etching for final metalization

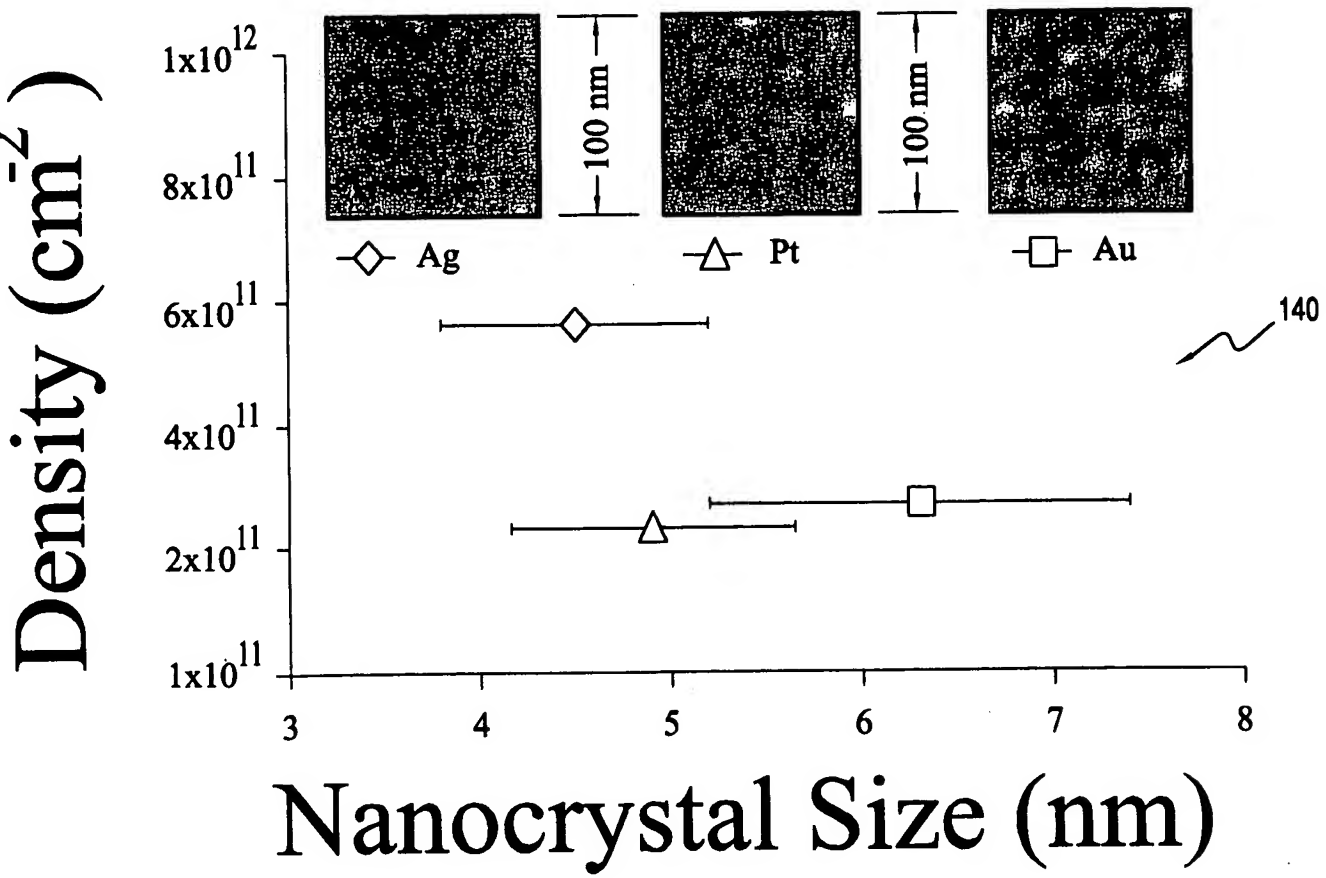


FIG. 13

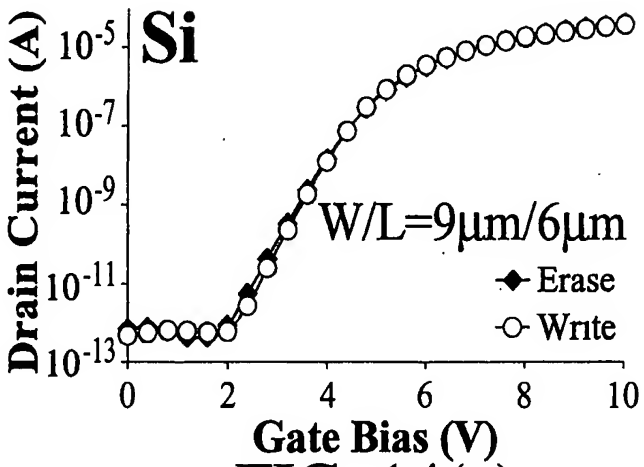


FIG. 14(a)

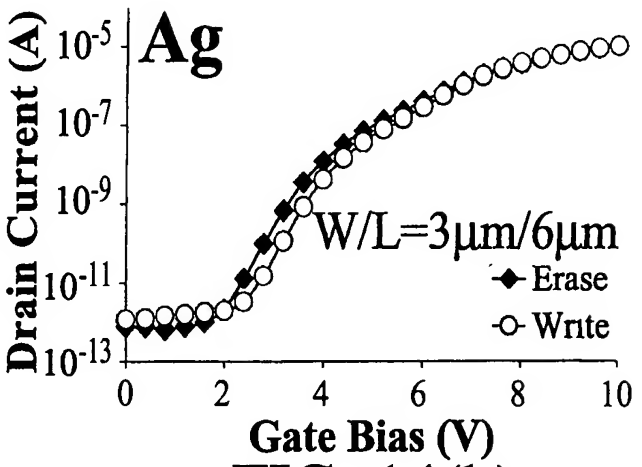


FIG. 14(b)

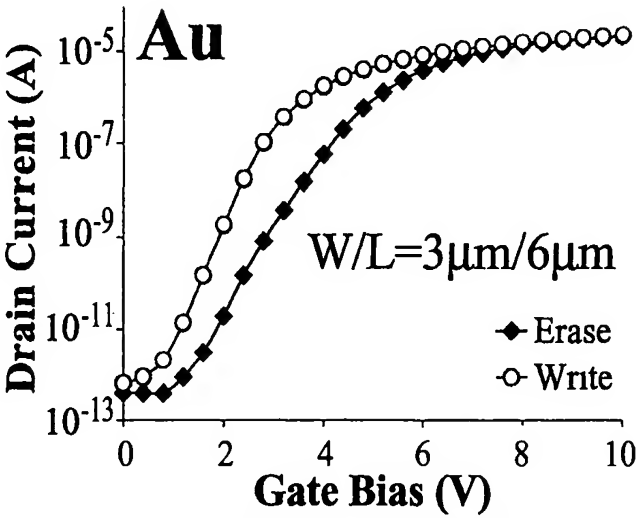


FIG. 14(c)

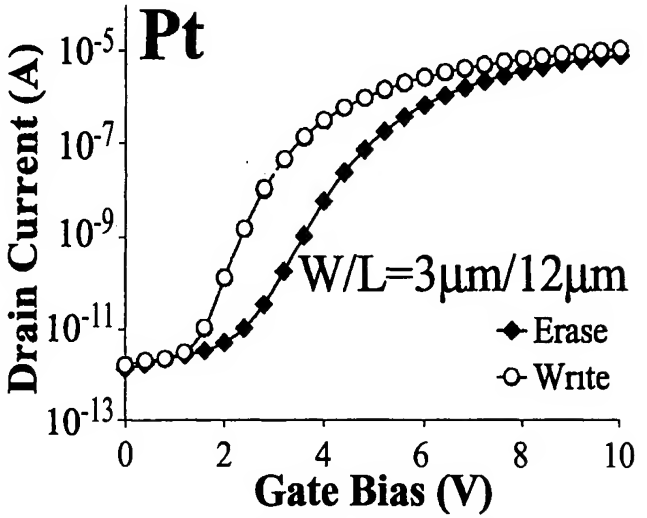


FIG. 14(d)

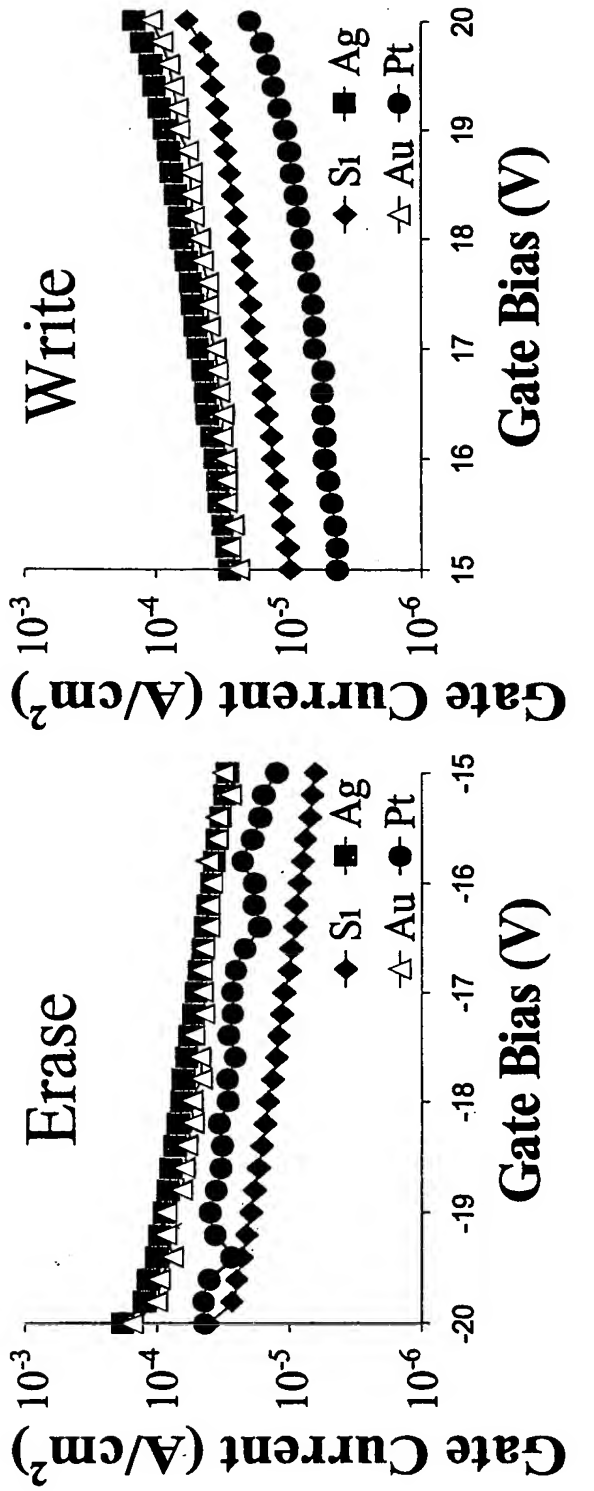


FIG. 15

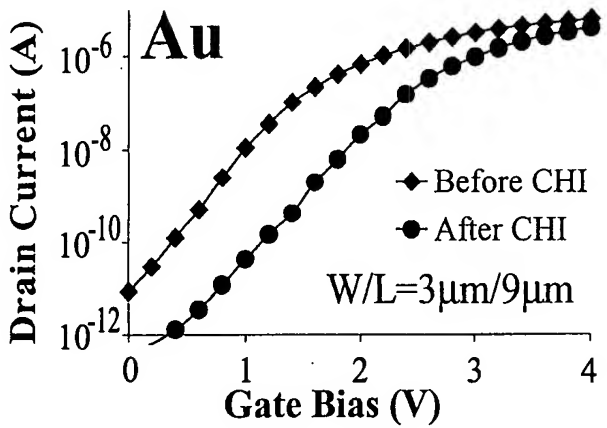


FIG. 16(a)

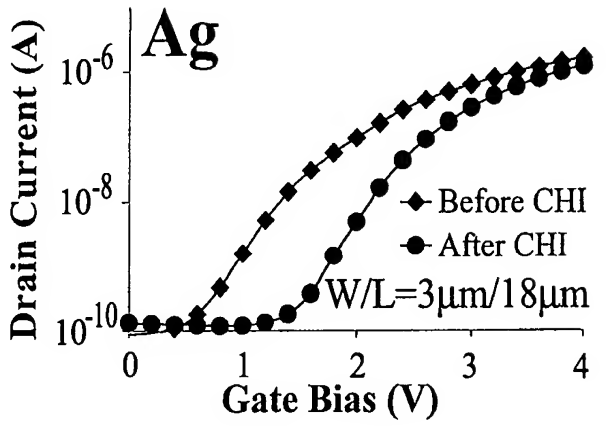


FIG. 16(b)

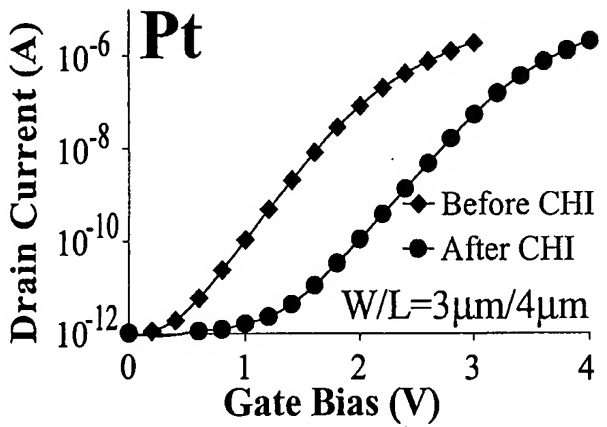


FIG. 16(c)

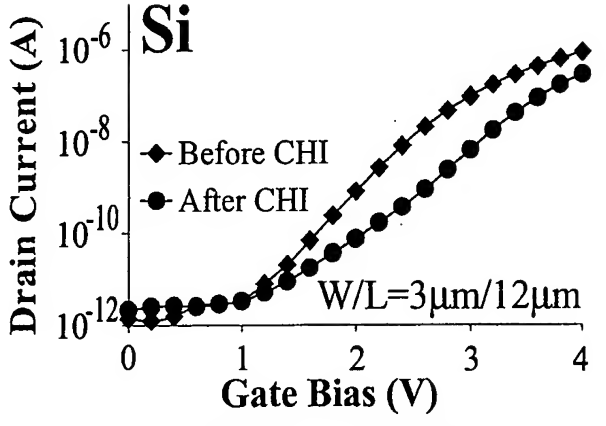


FIG. 16(d)

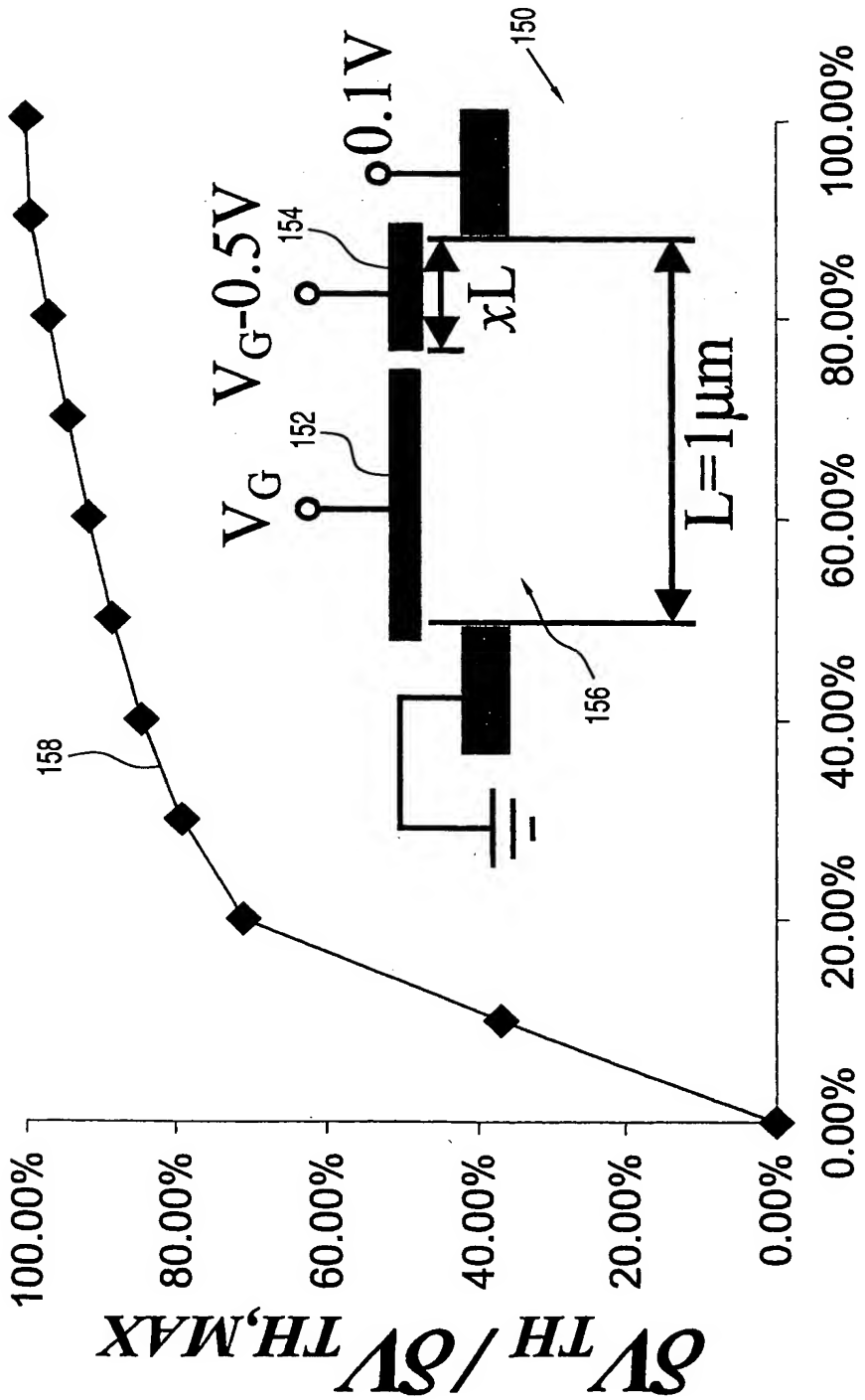


FIG. 17

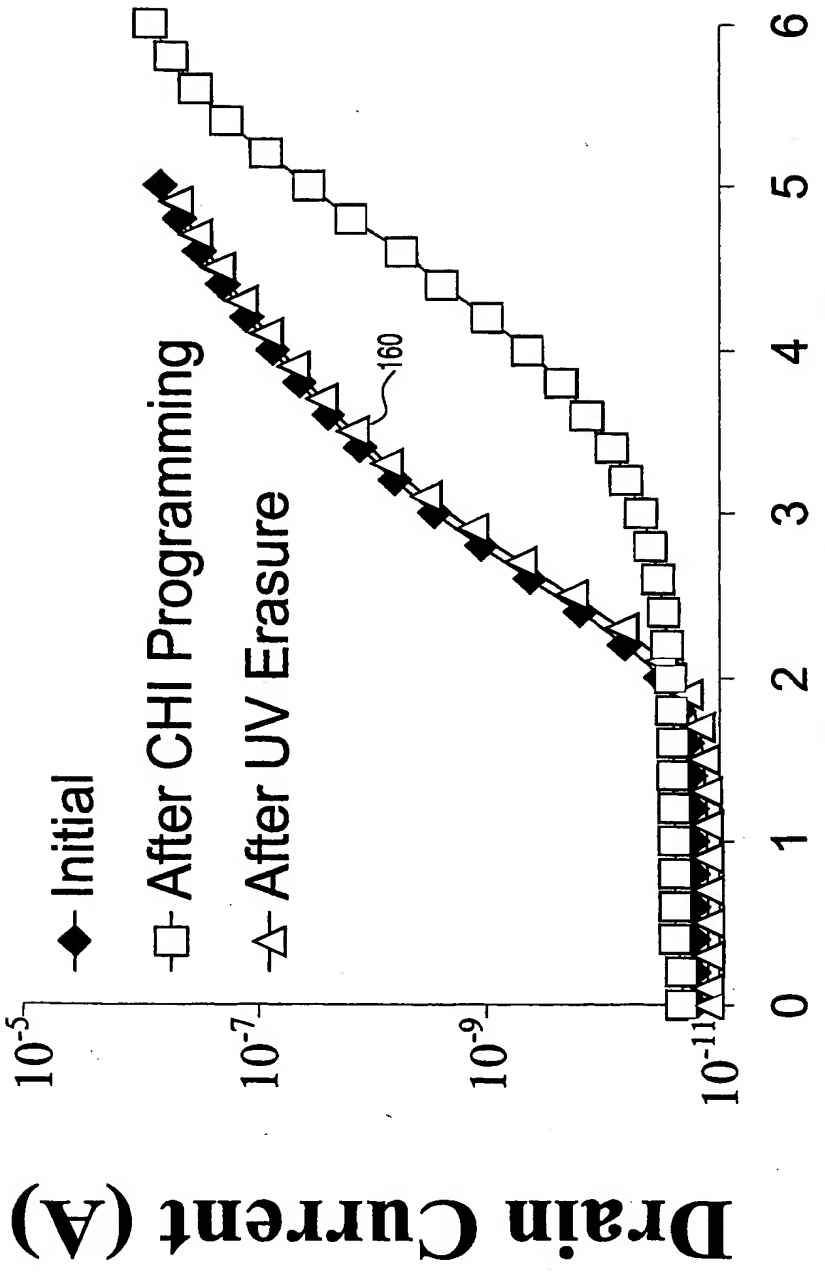


FIG. 18

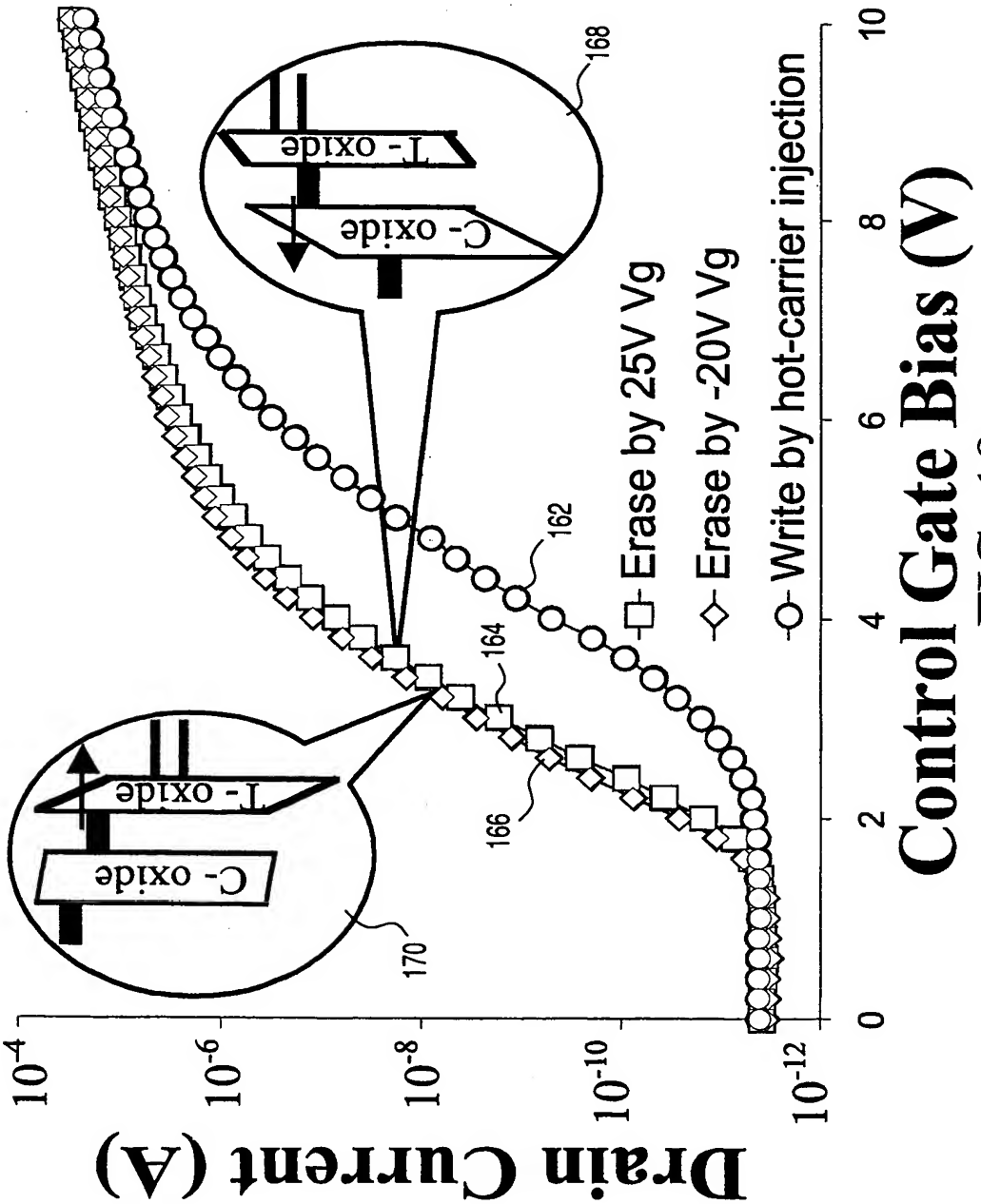


FIG. 19

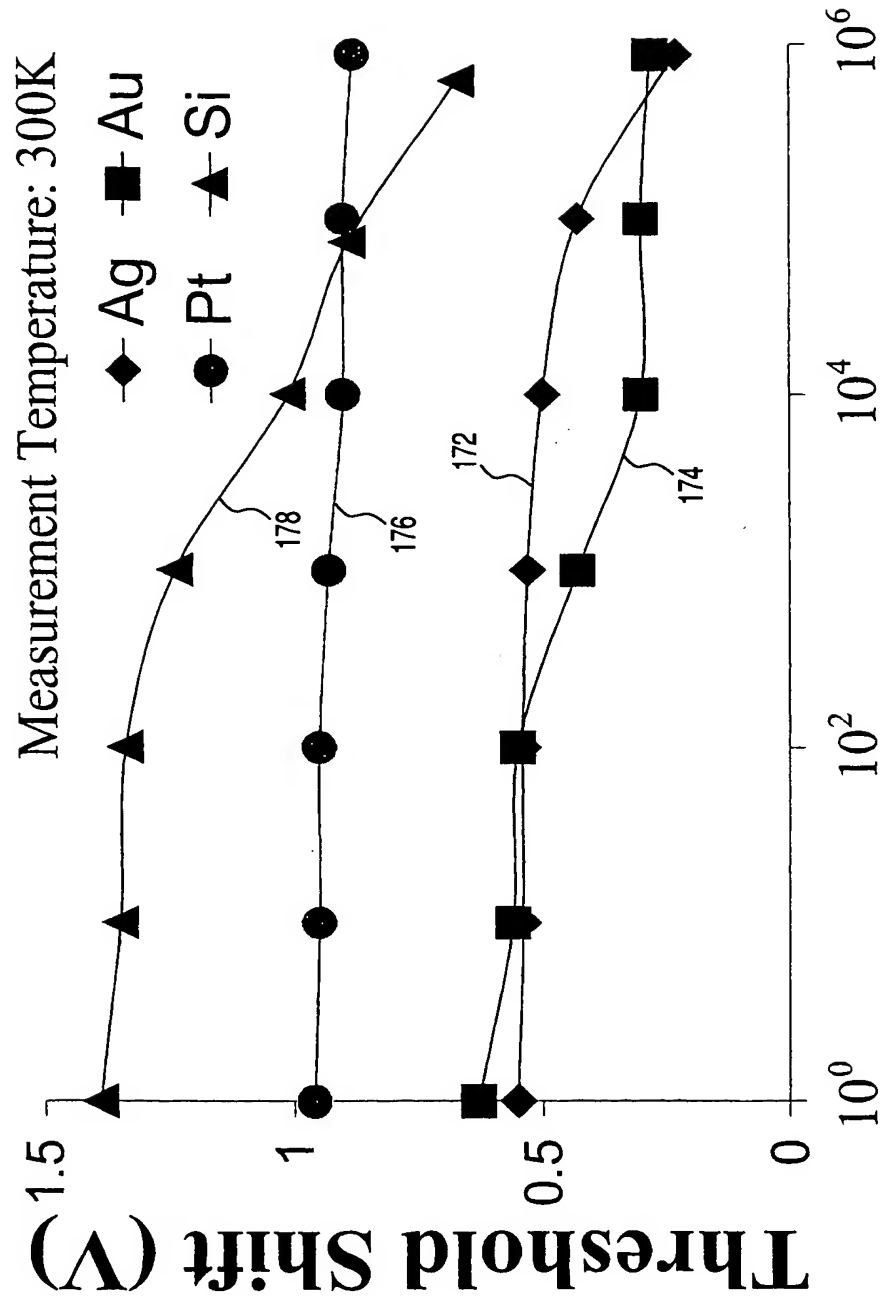
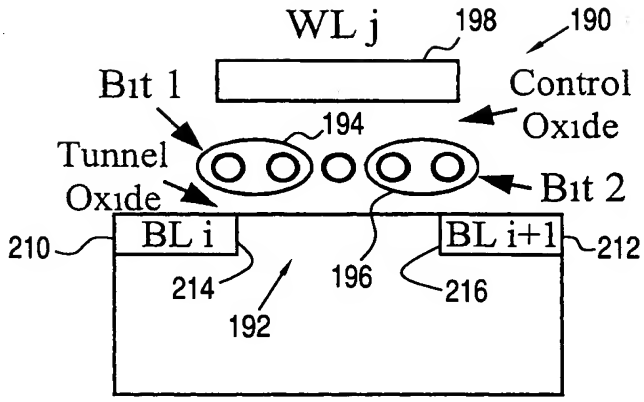
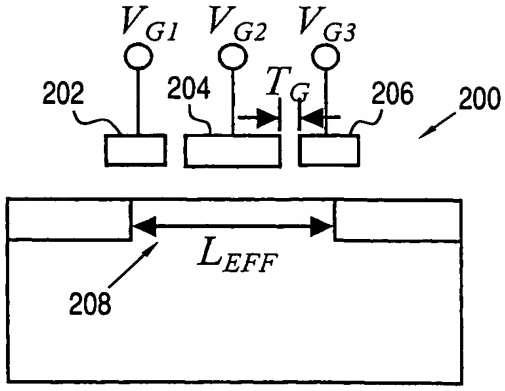


FIG. 20



Nanocrystal
Memory

FIG. 21(a)



Split-gate
MOSFET

FIG. 21(b)

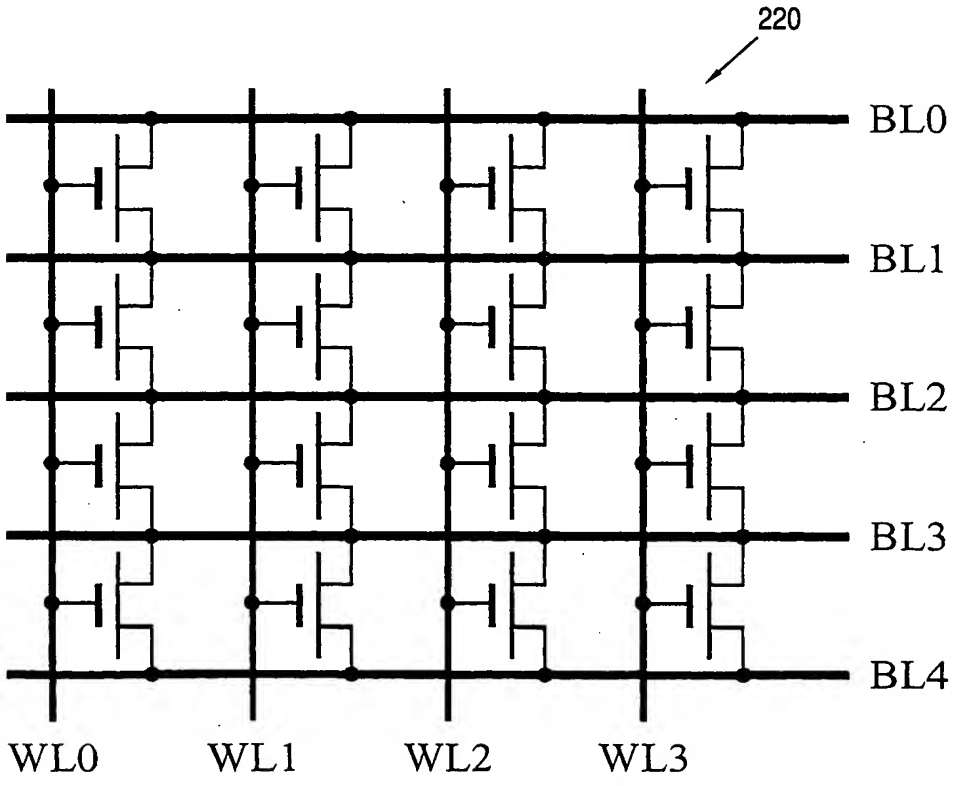


FIG. 21(c)

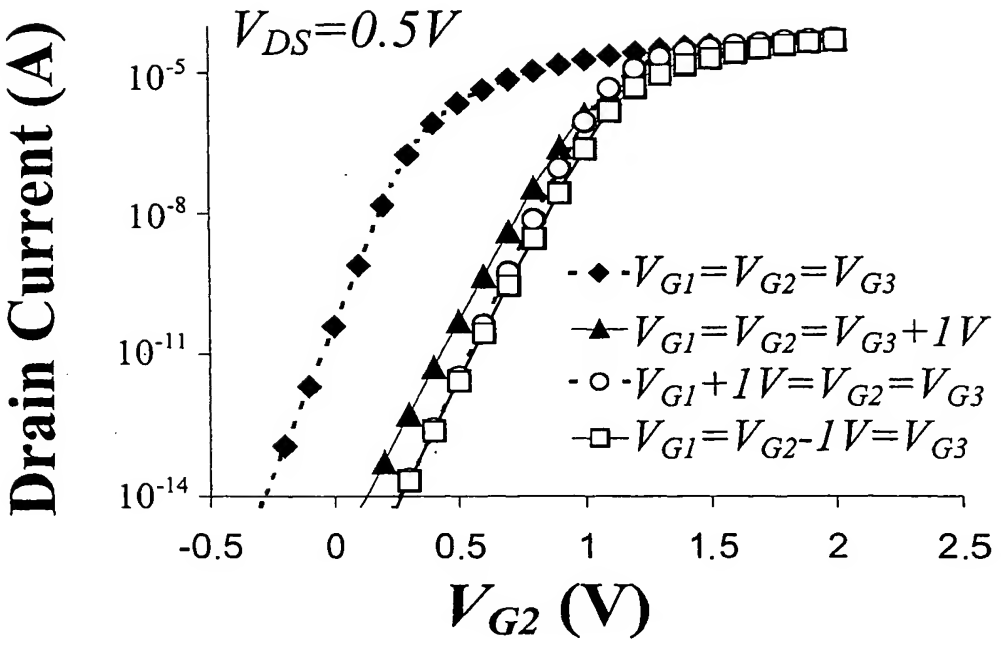


FIG. 22(a)

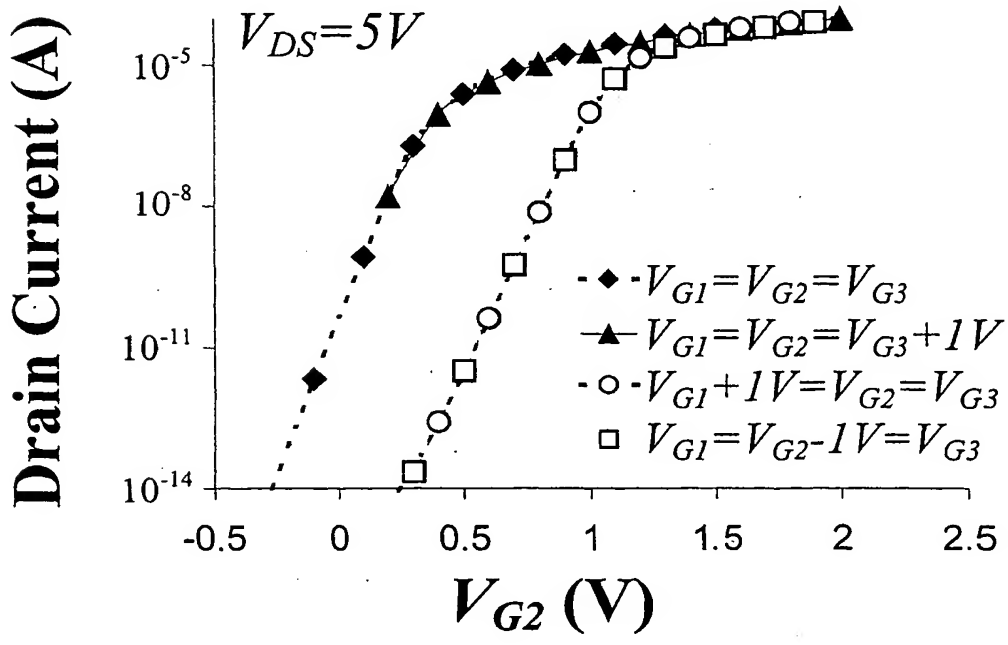


FIG. 22(b)

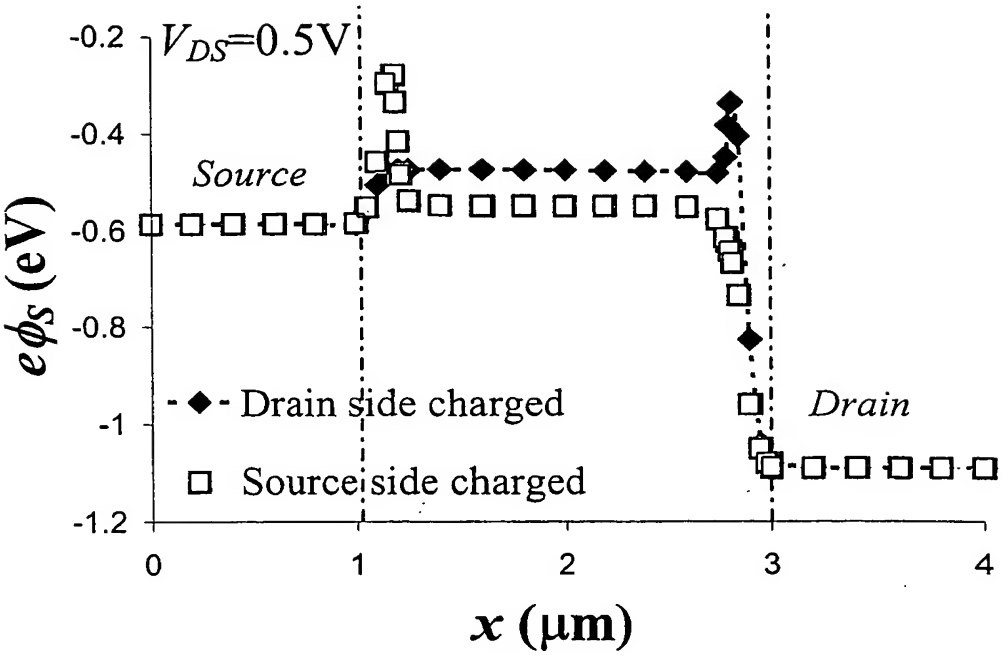


FIG. 23(a)

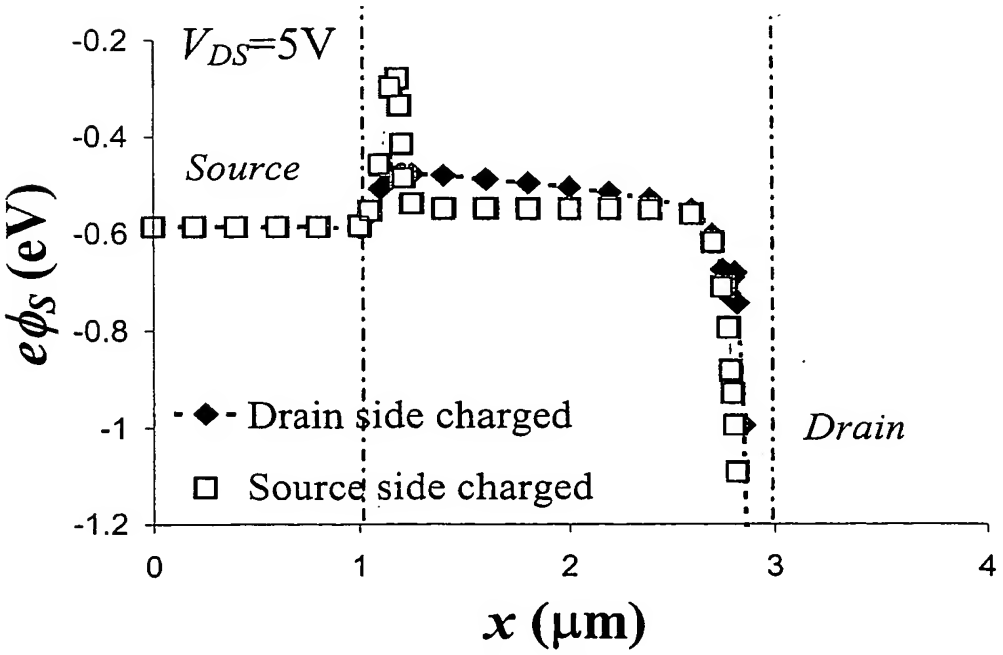


FIG. 23(b)

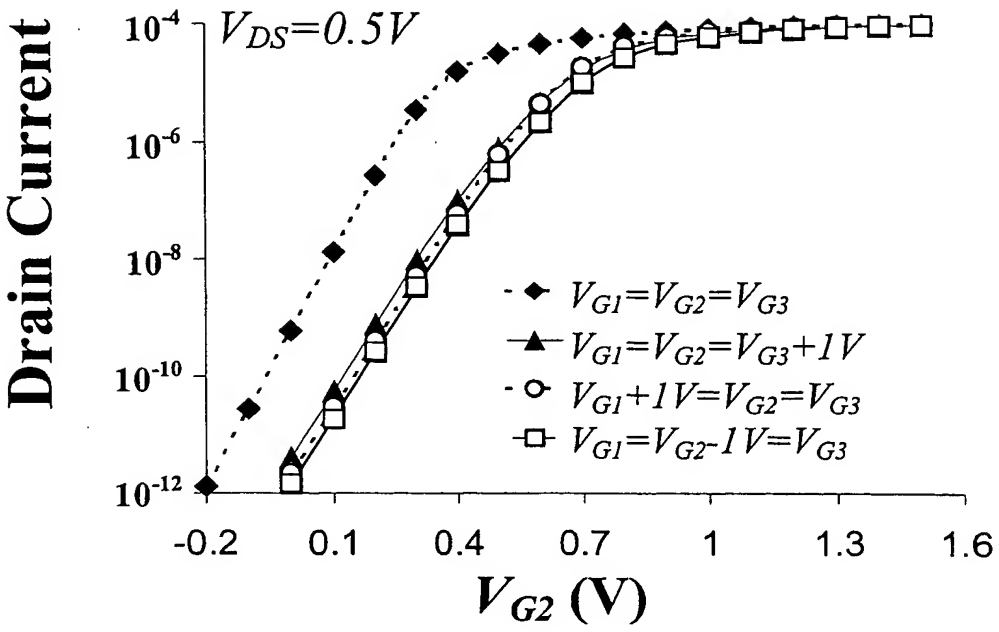


FIG. 24(a)

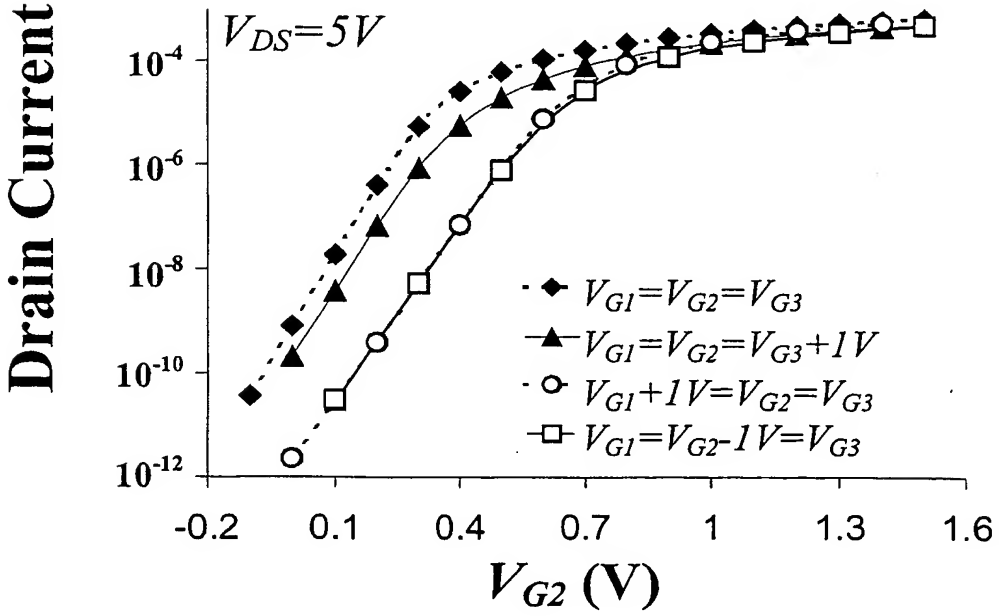


FIG. 24(b)

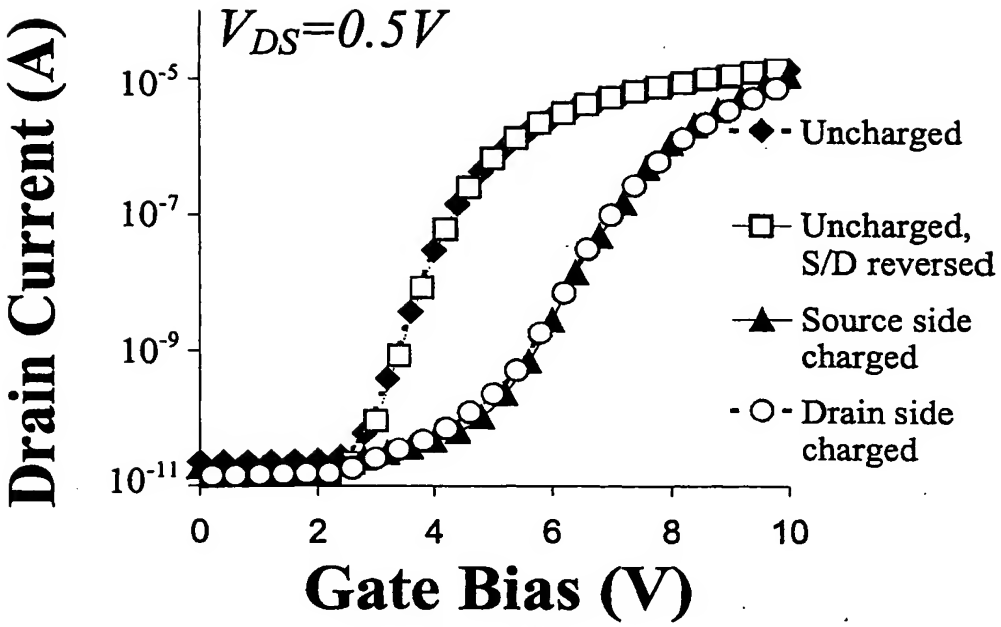


FIG. 25(a)

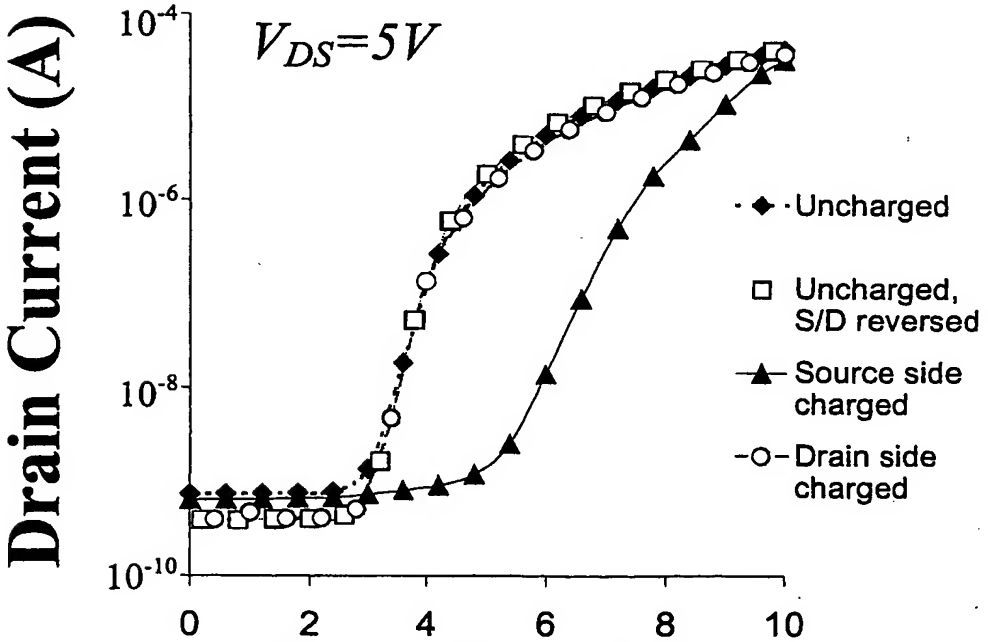
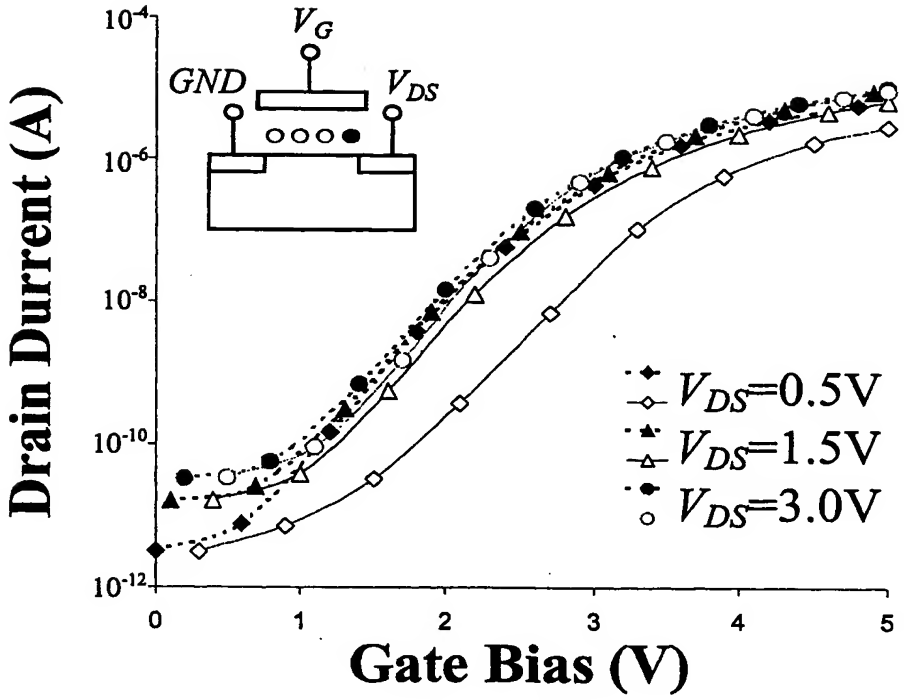
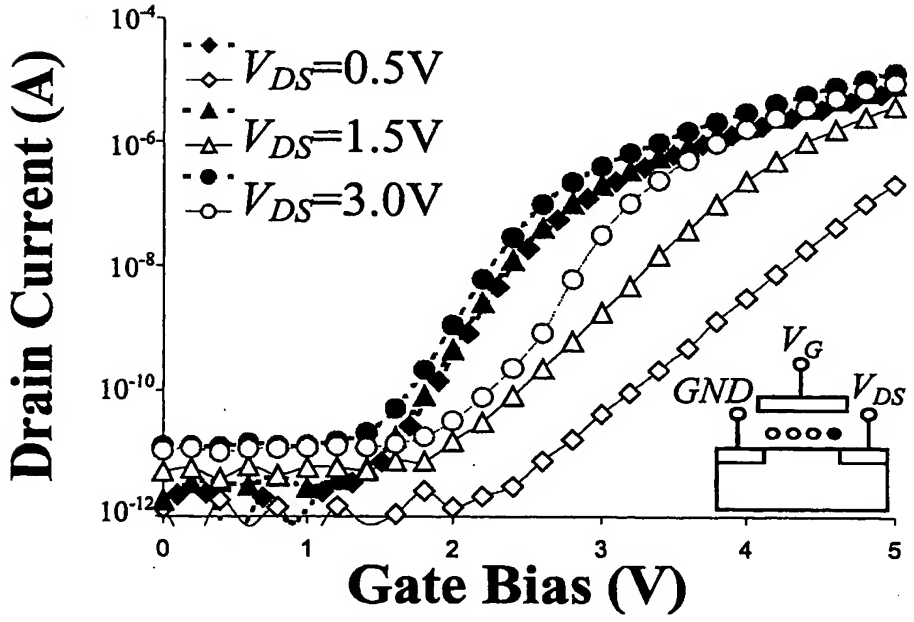


FIG. 25(b)



"Good cell"

FIG. 26(a)



"Overprogrammed cell"

FIG. 26(b)

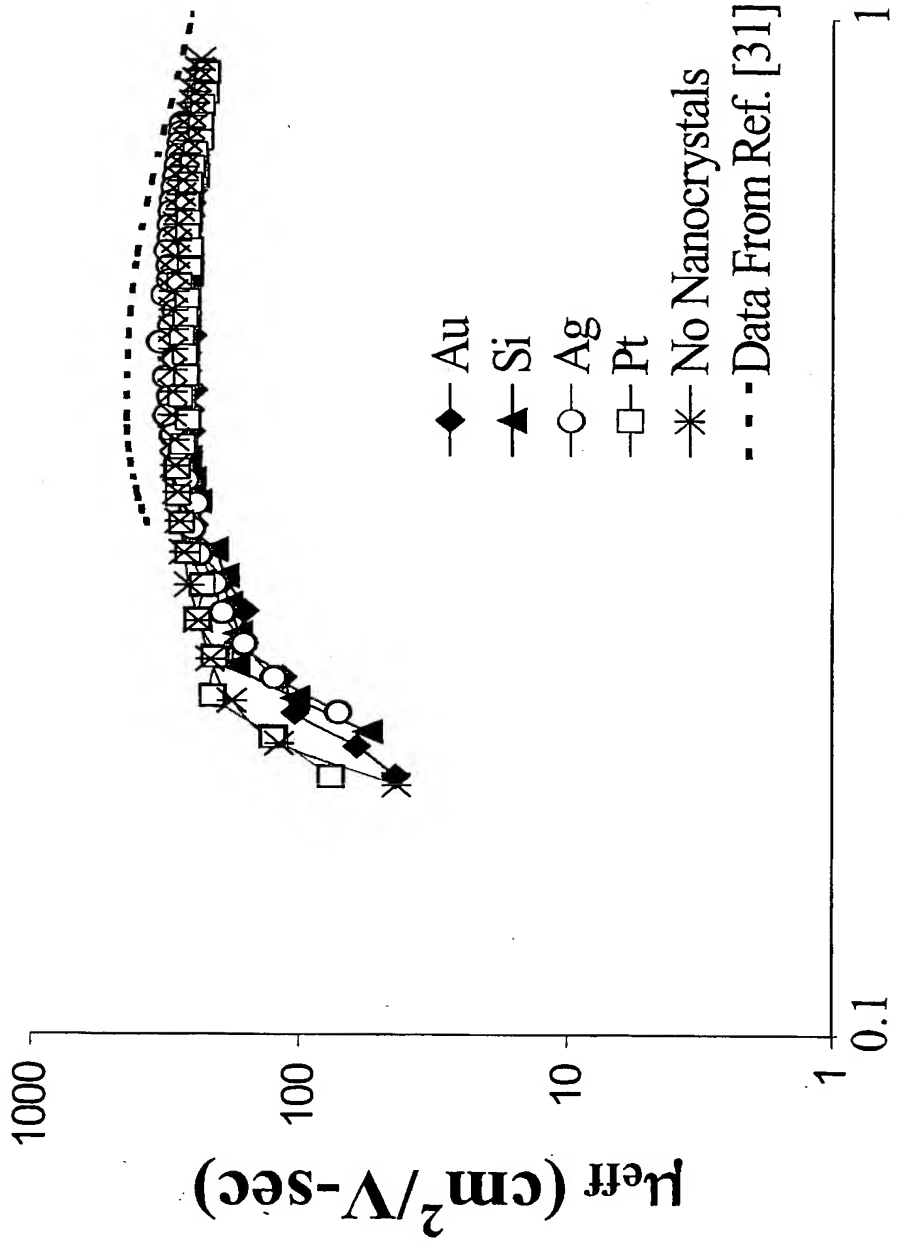


FIG. 27

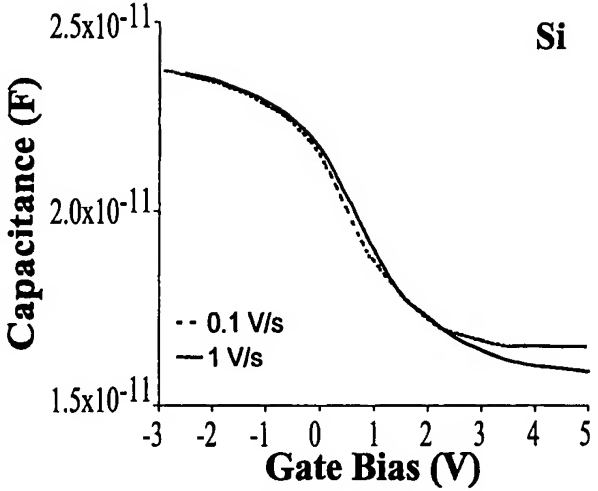


FIG. 28(a)

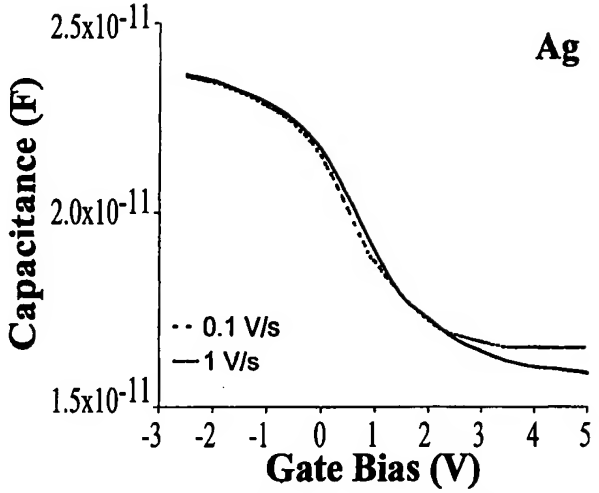


FIG. 28(b)

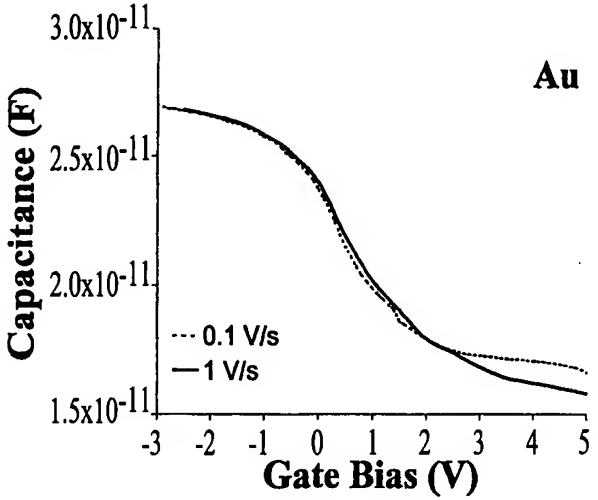


FIG. 28(c)

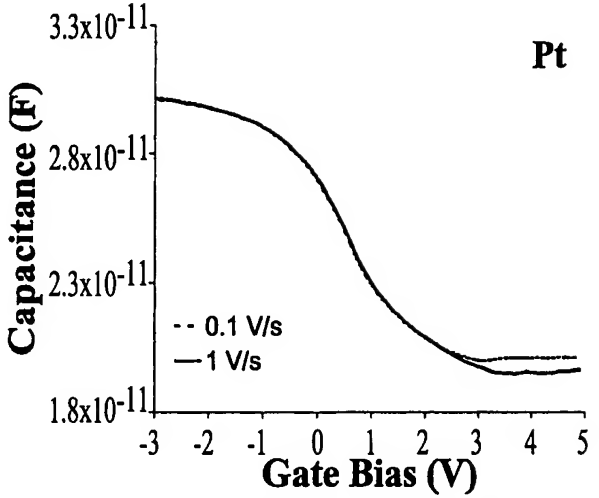


FIG. 28(d)